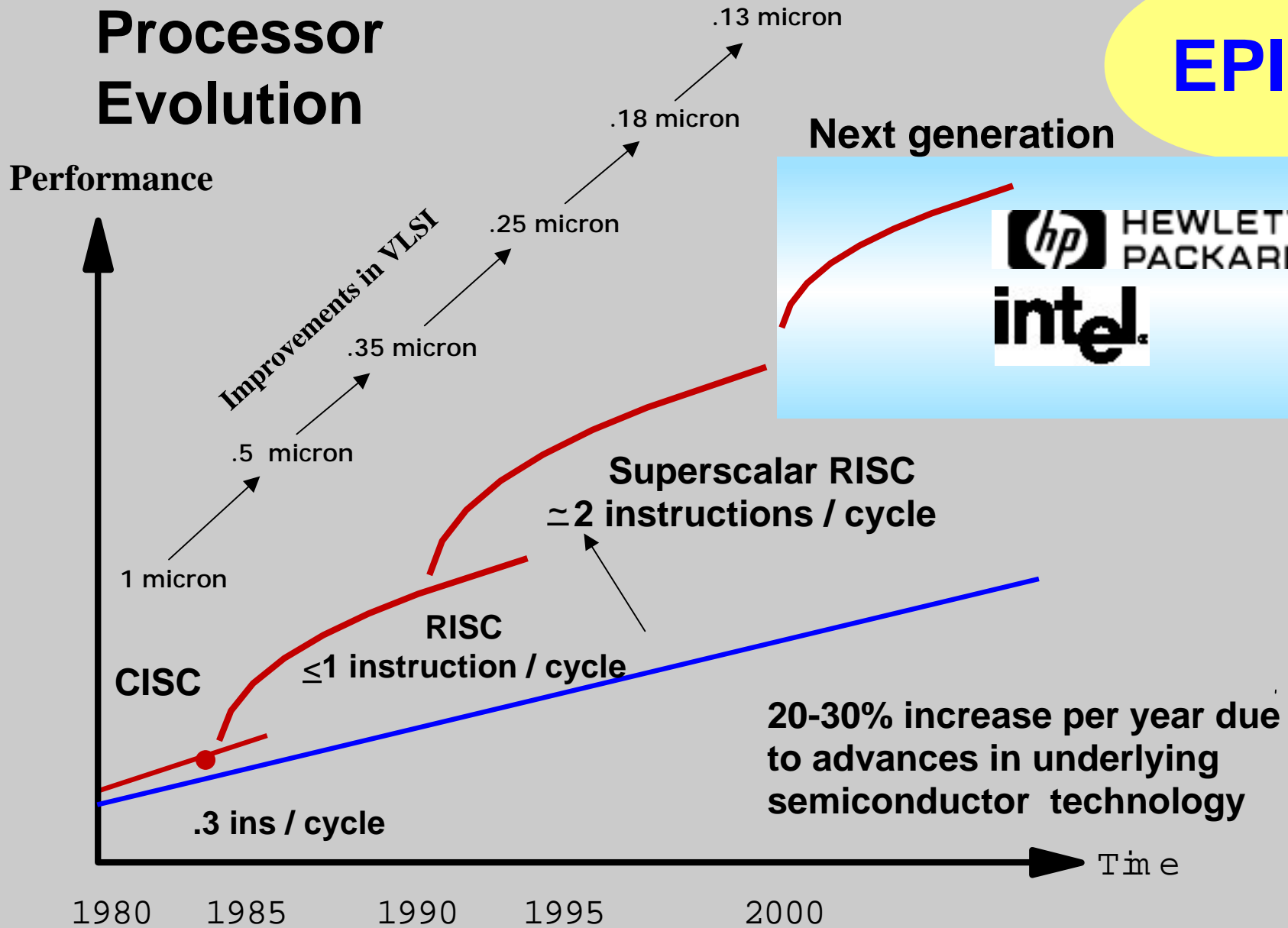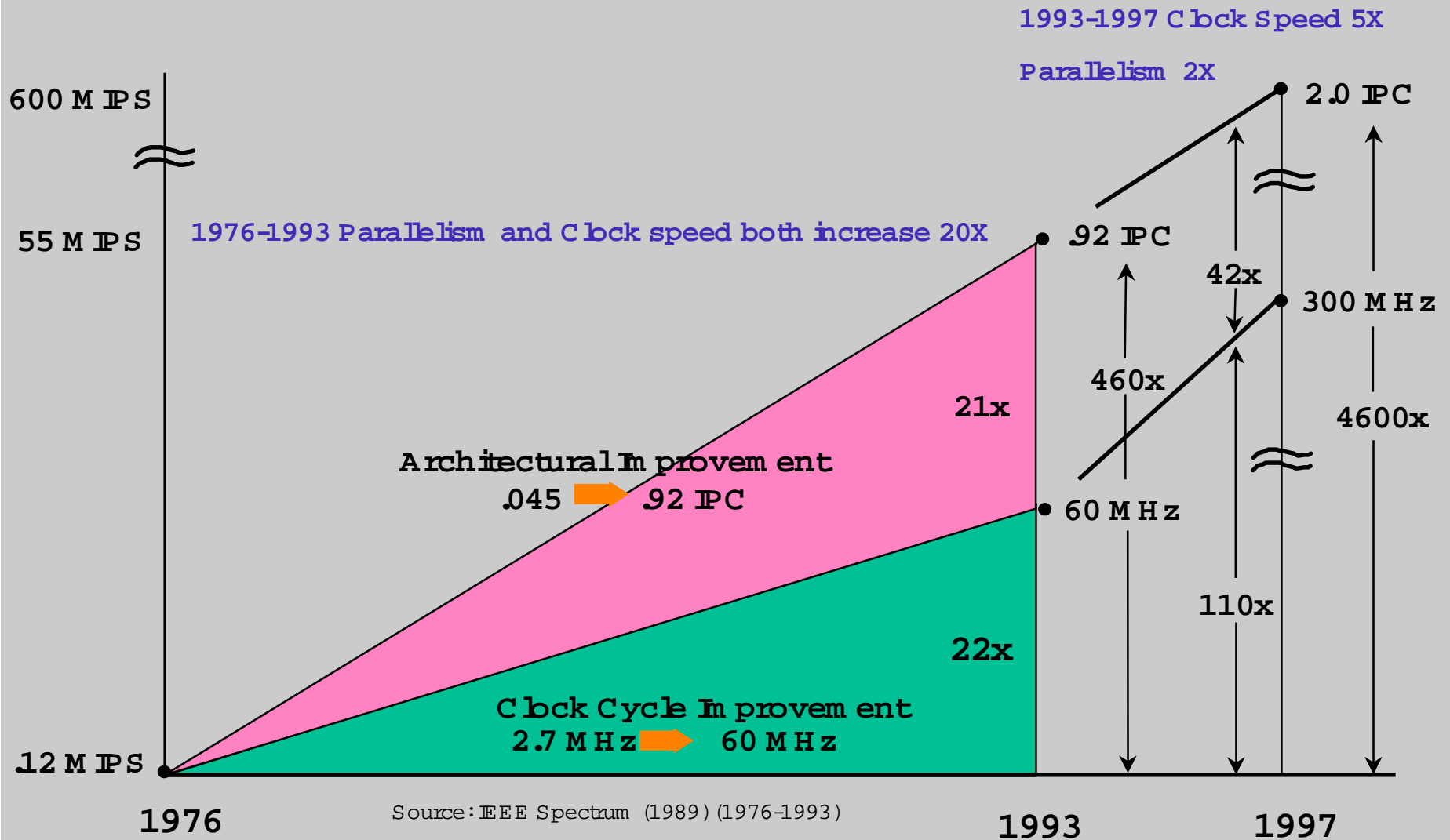# The Transition to IA-64

Ken Kroeker

Senior Technical Consultant

Partner Technology Access Center

Hewlett-Packard Company

120 Century Road West

Paramus, New Jersey

ken_kroeker@hp.com

Processor Evolution

Performance

EPIC

.13 micron

.18 micron

Next generation

.25 micron

Improvements in VLSI

.35 micron

.5 micron

Superscalar RISC
$\simeq 2$ instructions / cycle

1 micron

RISC
≤ 1 instruction / cycle

CISC

20-30% increase per year due to advances in underlying semiconductor technology

.3 ins / cycle

Time

1980   1985   1990   1995   2000

Microprocessor Performance Growth

1993-1997 Clock Speed 5X

Parallelism 2X

600 MIPS

2.0 IPC

1976-1993 Parallelism and Clock speed both increase 20X

55 MIPS

.92 IPC

42x

300 MHz

21x

460x

4600x

Architectural Improvement

.045 ➡ .92 IPC

60 MHz

22x

110x

Clock Cycle Improvement

2.7 MHz ➡ 60 MHz

.12 MIPS

1976

Source: IEEE Spectrum (1989) (1976-1993)

1993

1997

Today's Architecture Challenges

- Performance barriers :
    - Memory latency
    - Branches
    - Loop pipelining and call / return overhead
- Headroom constraints :
    - Hardware-based instruction scheduling
        - Unable to efficiently schedule parallel execution
    - Resource constrained
        - Too few registers
        - Unable to fully utilize multiple execution units
- Scalability limitations :
    - Memory addressing efficiency

IA-64 addresses these limitations

IA-64 Mission

- Overcome the limitations of today's architectures

- Provide world-class floating-point performance

- Support large memory needs with 64-bit addressing

- Protect existing investments
  - Full binary compatibility with existing IA-32 instructions in hardware
  - Full binary compatibility with PA-RISC instructions through software translation

- Support growing high-end application workloads
  - E-business and internet applications
  - Scientific analysis and 3D graphics

Define the next generation computer architecture

Architecting a Smooth Transition to IA-64

Hardware
- Parallel path of PA-RISC and IA-64
- IA-64-ready board upgradable systems

Operating system
- HP-UX is IA-64 ready (minor update)
- No administrator/operator interface changes
- Collaboration with Microsoft on NT transition
- HP Labs – first port of Linux to IA-64
- Simulators for early access to NT, Linux and HP-UX

Applications
- No forced application rewrites
- No data migration
- No forced applications recompiles
- PTAC for ISV Porting/Certification

PA-RISC will live on through IA-64

IA-64 retains many key PA-RISC characteristics:

- 1-to-1 mapping of performance-sensitive machine-level instructions
- PA-RISC virtual memory architecture
- Identical data formats
- PA-RISC floating point (IA-64 is a superset)
- PA-RISC multimedia (IA-64 is a superset)
- PA-RISC graphics acceleration
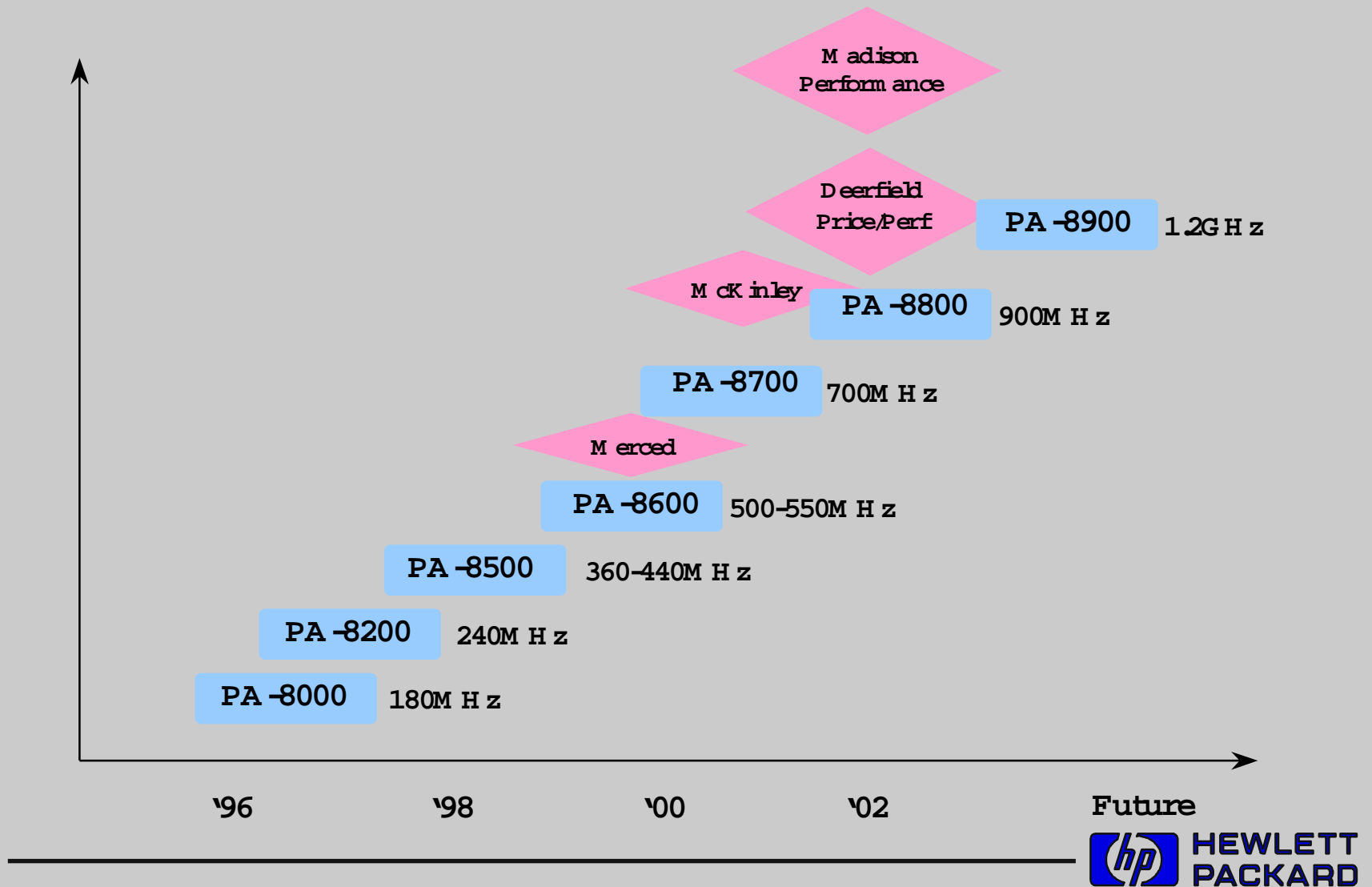- Many other features still kept confidential
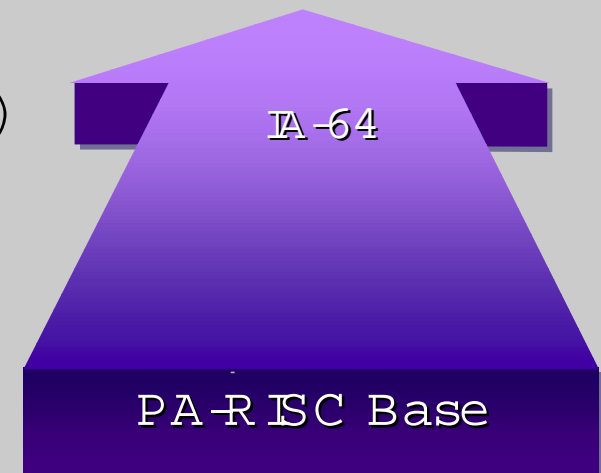
Benefits for PA-RISC customers:

IA-64

PA-RISC Base

- Smoother transition to IA-64 architecture designed in
- Easier ISV migration means more applications available sooner
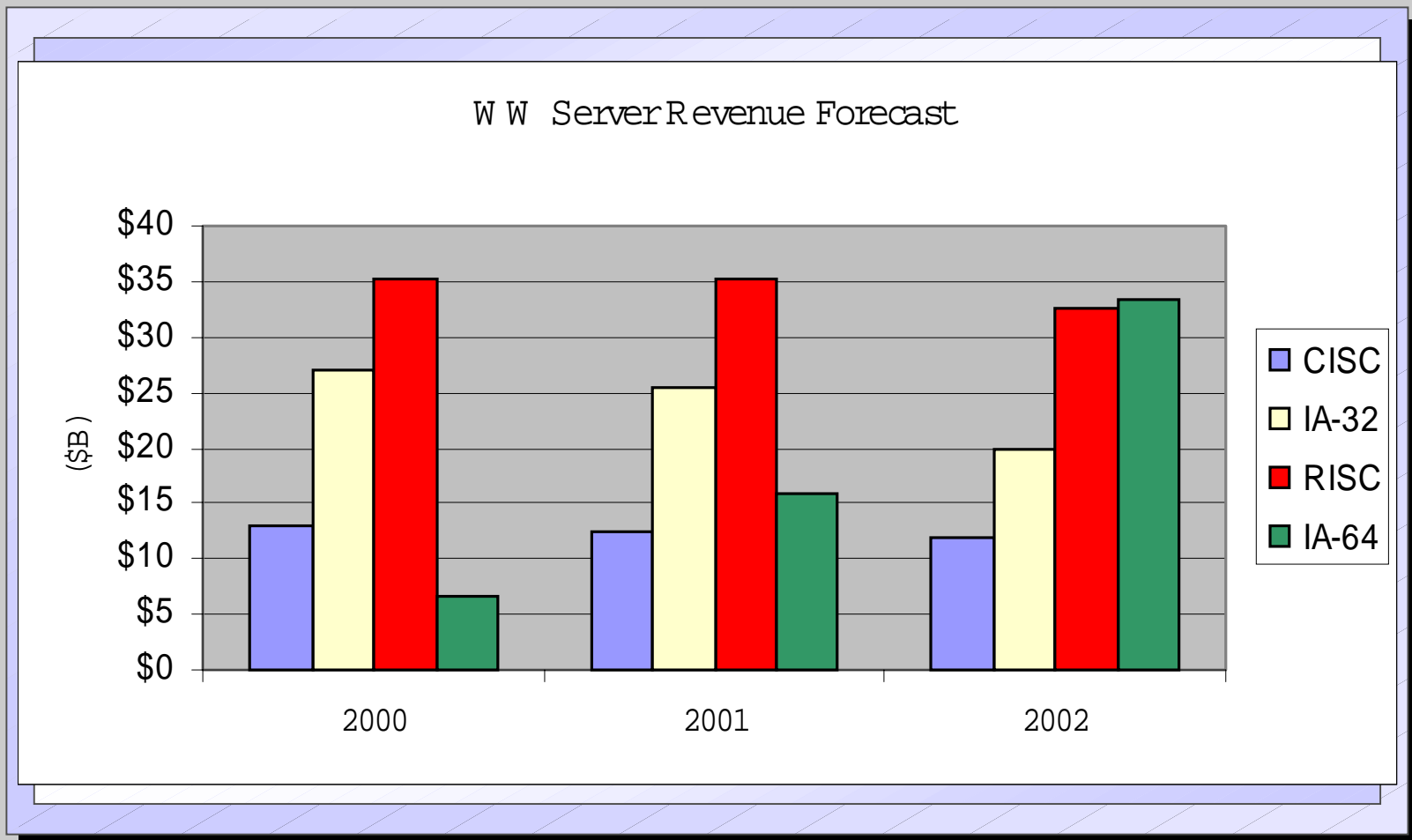- Better performance and reliability—functionality out sooner

Key: avoid "dead ends" where vendor can't move customers forward

HP Microprocessor Roadmap

Madison
Performance

Deerfield
Price/Perf

PA-8900   1.2GHz

McKinley

PA-8800   900MHz

PA-8700   700MHz

Merced

PA-8600   500-550MHz

PA-8500   360-440MHz

PA-8200   240MHz

PA-8000   180MHz

'96   '98   '00   '02   Future

HEWLETT
PACKARD

IDC Expects Rapid Rise of IA-64

WW Server Revenue Forecast

Source: IDC 5/98: "Hewlett-Packard Prepares for Rapid Rise of IA64-Based Systems"

Our Partners are Committed to IA-64

The software and Services you need when you need them !
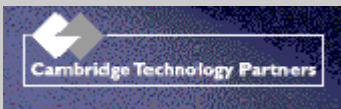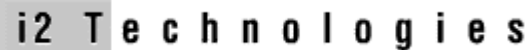
Transition Methods

Source Recompile

Binary Compatibility (transparent)

High-level Language (C, C++, FTN, Java, COBOL)

- Require recompilation
- Application Source Compatible
- Best performance
- C, C++ & FTN generate both 32 & 64 Bit code

PA Object Code

- Use Dynamic Translator technology
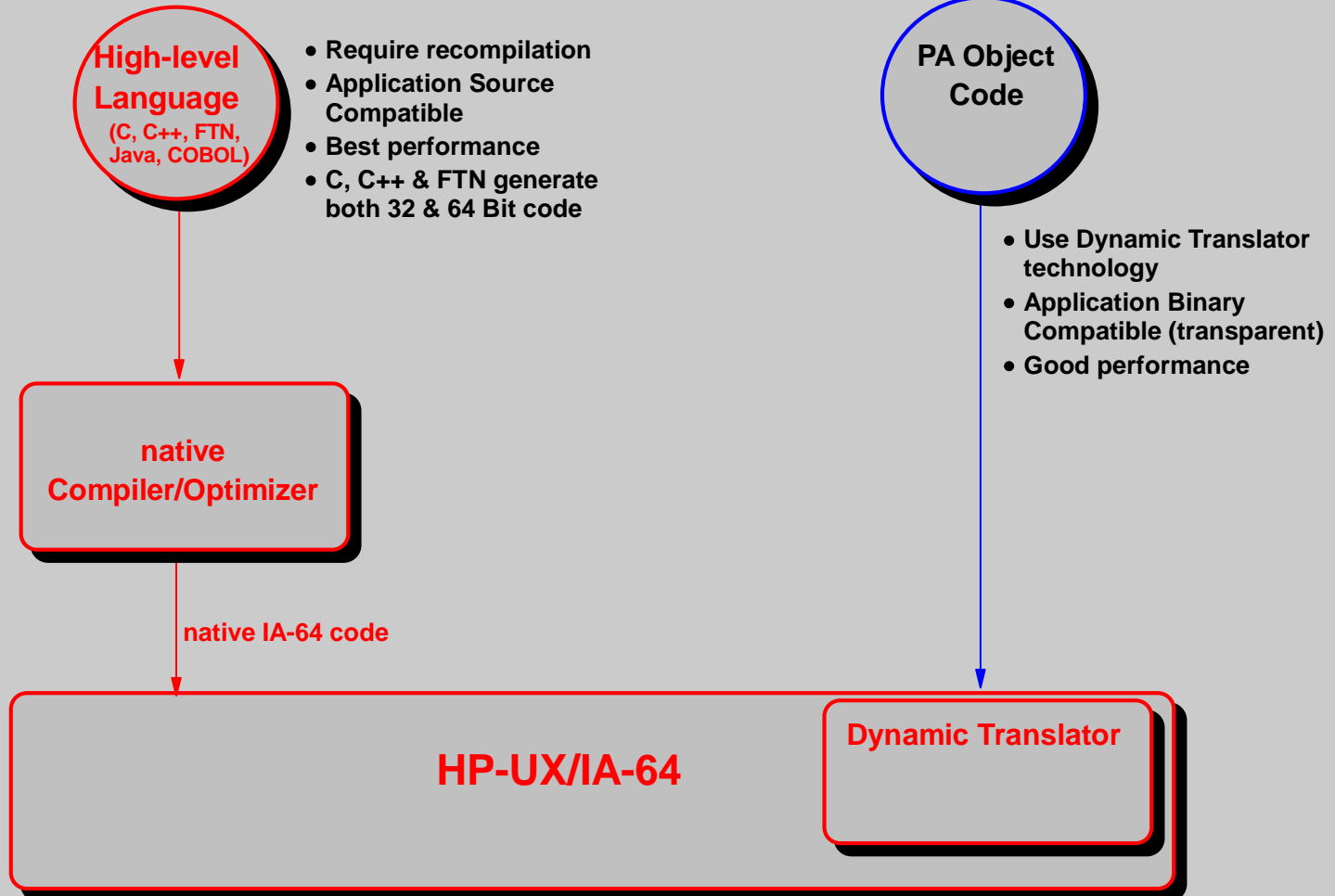- Application Binary Compatible (transparent)
- Good performance

native Compiler/Optimizer

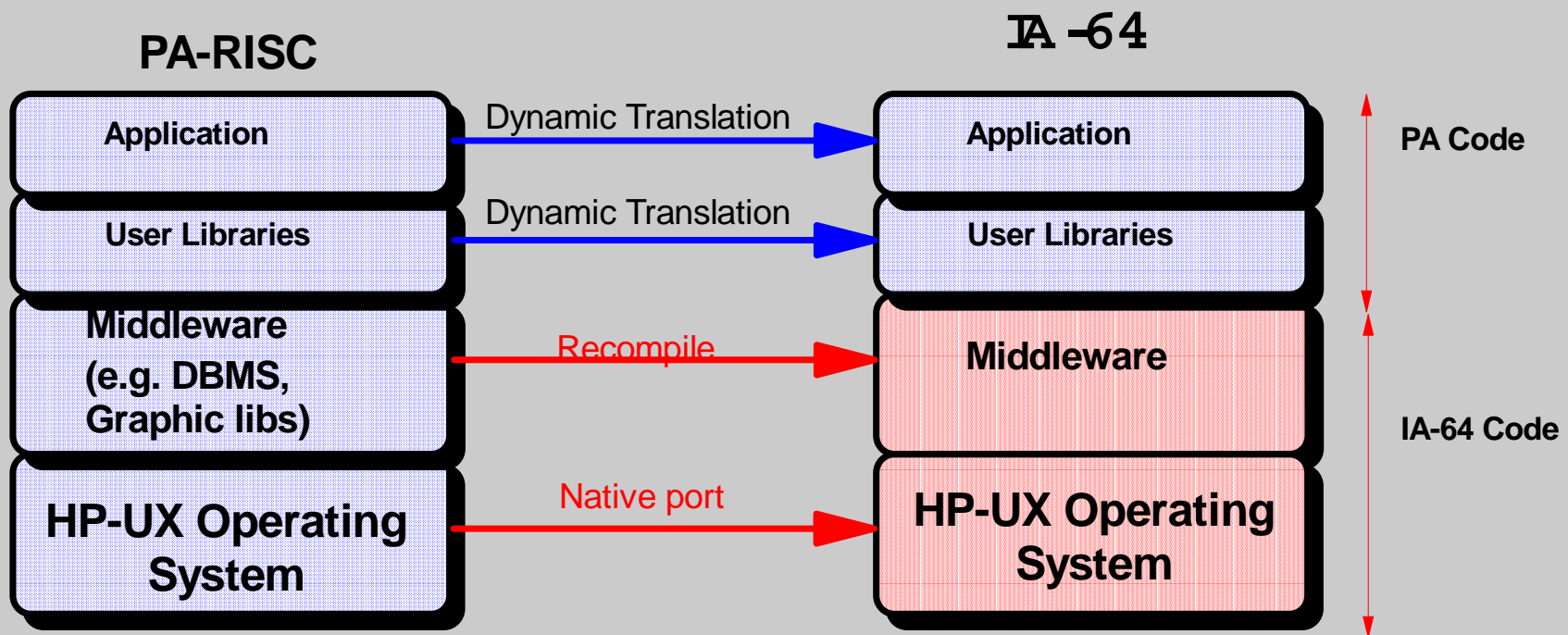native IA-64 code

HP-UX/IA-64

Dynamic Translator

Source Code Impacts

Potential Source Impacts
When Moving to IA-64

| From 9.X | From 10.01 | From 11.0 |
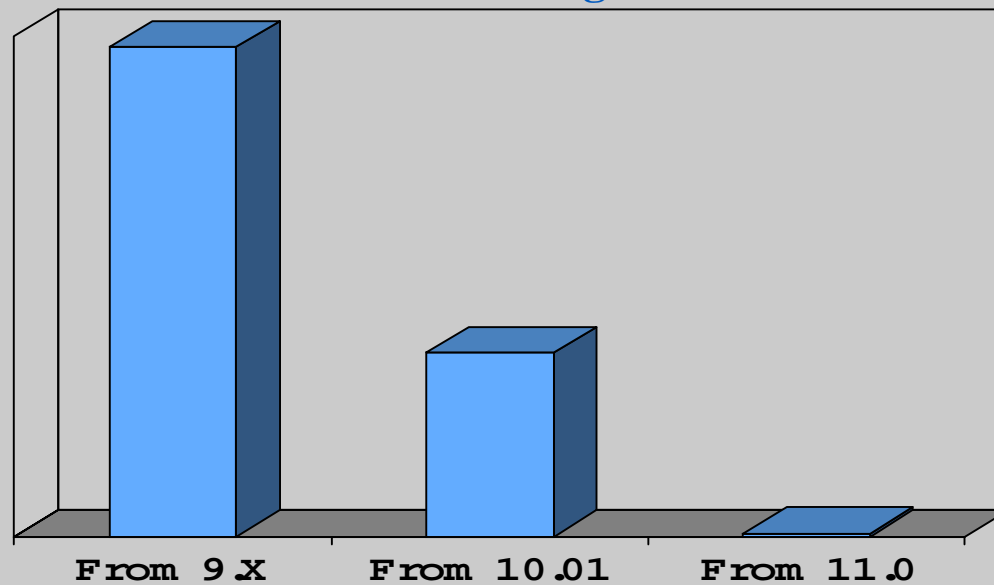
A clear jumping-off point

Execution Environment

- **A Mixed Environment**
- **Preserve the PA-RISC environment**
- **Allow incremental transition**

PA-RISC   **IA-64**

PA-RISC	IA-64	
Application	Dynamic Translation →	**Application**	PA Code
User Libraries	Dynamic Translation →	**User Libraries**	
Middleware (e.g. DBMS, Graphic libs)	Recompile →	**Middleware**	IA-64 Code
HP-UX Operating System	Native port →	**HP-UX Operating System**	

Dynamic Translation

- PA-RISC to IA-64 dynamic translator
- Features:
  - Highly reliable
  - Transparent
  - Good performance
  - Small set of limitations
- An integral part of HP-UX on IA-64, no installation required
- The Translator is user-level IA-64 code
- Invocation is automatic
- Optimization is unique to each execution

HEWLETT PACKARD

Full Binary Compatibility for PA-RISC

- **Transparency:**
  - Dynamic object code translator in HP-UX automatically converts PA-RISC code to native IA-64 code
  - Translated code is cached for later reuse
- **Correctness:**
  - Has passed the same tests as the PA-8500
- **Performance:**
  - Close PA-RISC to IA-64 instruction mapping
  - Translation on average takes 1-2% of the time Native instruction execution takes 98-99%
  - Optimization done for wide instructions, predication, speculation, large register sets, etc.
  - PA-RISC optimizations carry over to IA-64

Translator Limitations

- **If it doesn't run on the PA version of HP-UX 11.x, it won't run on IA-64 HP-UX 11.x**

- No mixing of PA and IA-64 components
  - PA executable w/ IA-64 shared libraries
  - IA-64 executable with PA shared libraries

- vfork acts like fork

- No support for privileged instructions, which means:
  - No kernel-intrusive codes
  - No device drivers
  - No home-grown operating systems

- No support for "/dev/kmem"

- No support for real-time or timing sensitive applications

- No support of signaling floating-point NaNs

- No support of ptrace and ttrace system calls

HEWLETT PACKARD

Impact on system

- The Translator installs a translated code cache for each PA process running on the IA-64 system in the application's stack area.

- An additional 1-8MB of swap space, depending on the size of the process and the swap-space pressure on the system, will be needed by the translator for each PA process

- IA-64 systems will easily run many hundreds of PA processes simultaneously

HEWLETT PACKARD

Translated Mode - Performance

- Databases, OS calls, IO will all be native code - Applications spending little of their time in user code will run with near Native mode performance

- Applications spending most of their time in the application code itself should be re-compiled

And Remember, Intel says:

- Mckinley will double Merced's performance at introduction
- Mckinley will be available at clock speeds >1Ghz

HEWLETT
PACKARD

What to look out for

Understand your environment - Do you really
know what code you run (A llof it) and where it
cam e from ... ..

Are you on HP-UX 11 X - If not, Get there.

Are you dependent upon any code for which
you do nothave the source, and for which no
IA-64 version is likely to be available -and is
thatcode perform ance sensitive?

There is no m ixed m ode. PA code cannotcall
IA-64 code and vice-versa. C lient server
im plem entations can getaround this.

Creating a Transition Plan

* **Take inventory**
  * **Ask your S/W vendors about their IA-64 plans**
  * **Confirm that your sources are really current**
  * **Take out the garbage**
* **If you are not there yet - Plan a transition to 11.0**
  * **Use HP services if necessary for 9.X -> 10.X**
  * **Use the 11.X STK to scan 11.X issues**
* **Understand your performance requirements**
* **Set Native mode transition priorities**
* **Can you keep running PA-RISC code (static apps?)**
* **Get help from HP or others if necessary**

Helping You Prepare for the Future

Documentation

HP-UX 9.x to 10.0 version B.10.01 Manual
9.X, 10.X, 11.X Release Notes
9.X to 10.X Transition Manual
11.0 Software Developers Guide
IA-64 CDROM
http://www.hp.com
http://software.hp.com/STK
http:/dtf.hp.com/dtf
http://www.hp.com/go/ia64

Tools

9.X ->10.X System Tools
9.X -> 10.X Application Tools
10.X -> 11.0 STK
11.0 -> 11.X (IA-64) STK
http://www.devresource.hp.com

Services

Response Center O.S. Upgrade Assistance Service
EPIC Readiness Services
Developer Alliances Lab
Designing the Future Seminars
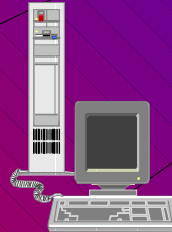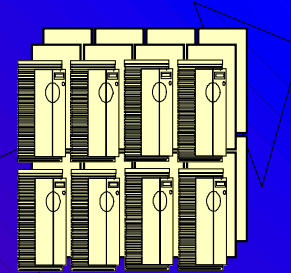*Customer Early Access Programs*

HEWLETT® PACKARD

Fut

PA-RISC and IA-64

- **Parallel with 2048 CPUs**
- **PCI I/O**

- **1-64W SMP**
- **PCI I/O**

- **1-8W SMP**
- **PCI I/O**

- **1-4W SMP**
- **PCI I/O**

What Do We Know About IA-64 and the HP 3000?

➡ New comparably performing PA-RISC processors are being introduced through 2002/2003

➡ IA-64 MPE/iX will require a separate release

➡ User PA-RISC applications will not have to be recompiled

➡ CSY's goal is to allow Classic HP 3000 binary code to run, unrecompiled on IA-64 HP 3000 Servers

➡ Recompiled Classic and PA-RISC applications will run faster

➡ Next generation servers will be board upgradeable to IA-64

➡ MPE/iX support of IA-64 will occur beyond 2001

➡ When IA-64 MPE/iX is introduced, PA-RISC MPE/iX will continue to be supported in parallel

Stay tuned for more details